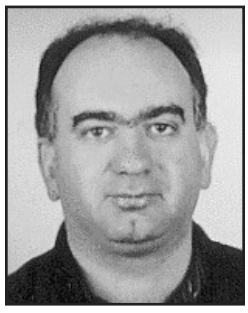
Session 22 Overview

Digital Circuit Innovations



Chair: David Blaauw, *University of Michigan, Ann Arbor, MI*

Associate Chair: Georgios Konstadinidis, *Sun Microsystems, Sunnyvale, CA*

Last year at ISSCC, a panel hotly debated the question "is the digital designer is dead?" Counter to some of the voiced opinions at this panel, this session demonstrates vibrant innovation in the area of digital circuits. These innovations address a number of challenges that have emerged in 65nm technology that are stressing existing circuit design practices. For instance, the analysis and control of process variation has come to the forefront of digital design. Device performance has become increasingly unpredictable due to process variations, sensitivity to temperature and supply voltage, and life-time wear-out mechanisms, such as oxide breakdown and negative-bias temperature instability (NBTI). To address this looming challenge, four papers in this session propose techniques that measure and adjust to variations. While these papers resist the consequences of variation, two other papers actually exploit variation to create random numbers for security applications.

In addition to the increase in variation, dynamic and static power consumption are concerns that must be addressed by today's circuit designers. The slowdown of supply-voltage reduction in the nanometer era, combined with continuing scaling has resulted in tight power-constraints for digital circuit designs. A significant component of the total power consumption resides in global wires. Hence, the final two papers in this session present approaches for high-speed on-chip communication with substantially reduced power consumption.

In Paper 22.1, IBM introduces a delay-measurement sensor to monitor the critical path delays, which can be used to optimize the performance across voltage, process and the operational life time, in the face of wearout mechanism. Results are reported for a commercial 65nm POWER6 processor. Paper 22.2 from IBM and Purdue U addresses the need for characterizing process variations in advanced processes. An integrated array of sense amplifiers allows efficient statistical characterization of random dopant fluctuations for different types of devices. A self-adjusting circuit that addresses variations and chip wearout is presented in Paper 22.3 from NEC. The method employs in-situ delay monitoring latches for the critical paths and proactively reconfigures the circuit to avoid impending failures.

Papers 22.4 from U Michigan and Paper 22.5 from U Washington both present different methods for random number generation for security applications. The method in Paper 22.4 uses meta-stability to generate and grade the quality of a continuous stream of true random numbers. In Paper 22.5 introduces a new method that produces a random but fixed string of bits for chip ID applications.

Paper 22.6 from Korea U and Hynix addresses variation by introducing an output driver that uses on-die delay measurement to control slew rates and dynamically compensate for noise and process variations.

Paper 22.7 from Sun Microsystems discusses a state-of-the-art TLB design for the Niagara-2 processor, addressing the design challenges in 65nm process and in multi-core and multi-threaded processing.

The final two papers in the session, Paper 22.8 from Sun Microsystems and Paper 22.9 from U Twente, introduce a new method for high speed on-chip interconnects. Both methods use a capacitively-coupled driver which produces both pre-emphasis and small signal swings, leading to significant interconnect power reduction.

22.1 A Distributed Critical-Path Timing Monitor for a 65nm High-Performance Microprocessor **8:30 AM**

A. Drake, IBM, Austin, TX

A distributed critical-path timing monitor (CPM) is designed as part of the POWER6™ microprocessor in 65nm SOI. The CPM is capable of monitoring timing margin, process variation, localized noise and V_{DD} droop, or clock stability. It tracks critical-path delay to within 3 FO2 delays at extreme operating voltages with a standard deviation less than 1/2 an FO2 delay. The CPM detects DC V_{DD} droops greater than 10mV and tracks timing changes greater than 1 FO2 delay.

22.2 Statistical Characterization and On-Chip Measurement Methods for Local Random Variability Using Sense-Amplifier-Based Test Structure **9:00 AM**

S. Mukhopadhyay, IBM T.J. Watson, Yorktown Heights, NY, and Purdue University, West Lafayette, IN

An on-chip digital characterization method for local random variation in a process is presented. The method uses a sense-amplifier-based test circuit that uses digital voltage measurement instead of the analog current measurements of conventional techniques. The proposed circuit helps design fast on-chip built-in-self-test schemes for measuring random variation. A testchip is designed in 0.13µm CMOS and measured to show the effectiveness of the proposed circuit in extracting local random variation.

22.3 Fine-Grain Redundant Logic Using Defect-Prediction Flip-Flops **9:30 AM**

T. Nakura, NEC, Kanagawa, Japan

Chip production yield of 70% can be increased to 91% by using fine-grain redundant logic in which only the defective portion of the main circuit is switched to a redundant subcircuit block. In addition, defect-prediction flip-flops prevent over 80% of in-field failures caused by latent defects, while maintaining correct operation. All flip-flops are connected via a scan chain, which can be employed to reproduce states used in avoiding defects, and to trace defect points.

22.4 True Random Number Generator with Metastability-Based Quality Control **10:15 AM**

C. Tokunaga, University of Michigan, Ann Arbor, MI

A proposed metastability-based true random number generator (TRNG) achieves high entropy and passes NIST randomness test by grading the randomness of each metastable event through the measurement of its resolution time, regardless of the output bit value. This allows the system to determine the original noise level at the time of metastability and to tune itself for maximum randomness. A fully integrated 0.036mm^2 TRNG is fabricated and measured in a 0.13µm technology.

22.5 A 6.3pJ/b 96%-Stable Chip-ID Generating Circuit Using Process Variations **10:45 AM**

Y. Su, University of Washington, Seattle, WA

A 128b 6.3pJ/b, 96%-stable chip-ID generation circuit using process variation is designed in a 0.13µm CMOS technology. The circuit consumes 162nW from a 1V supply at low readout frequencies and 6.34µW at 1Mb/s. Two layout techniques are designed and fabricated to provide a performance comparison of power consumption and ID reliability.

22.6 A One-Cycle Lock Time Slew-Rate-Controlled Output Driver **11:15 AM**

Y-H. Kwak, Korea University, Seoul, Korea

A low-power output-on-demand slew-rate-controlled output driver is presented. It has an open-loop digital scheme and a one-cycle lock time applicable to high-speed memory interfaces. The output driver maintains slew rate between 2.1V/ns and 3.6V/ns for the SSTL interface. Fabricated in a 0.18µm CMOS process, the control block of the proposed driver occupies 0.009mm^2 and consumes 13.7mW at 1Gb/s. No external resistance is needed to calibrate the output resistance of the output driver.

22.7 A Single-Cycle-Access 128-Entry Fully-Associative TLB for Multi-Core Multi-Threaded Server-on-a-Chip **11:30 AM**

S. Shastry, Sun Microsystems, Sunnyvale, CA

A single-cycle-access, 128-entry fully-associative multi-context TLB was designed for the Niagara2 SPARC™ processor in 65nm triple-V_t 11M 1.1V CMOS. The circuit includes a dual-storage CAM cell, a modified dual matchline, an 8T 1-read/1-write based RAM, 4-way comparators for cache hit, a priority encoder, a multi-match detect, and data parity.

22.8 High-Speed and Low-Energy Capacitively-Driven On-Chip Wires **11:45 AM**

R. Ho, Sun Microsystems, Menlo Park, CA

Capacitively-driven on-chip wires reduce both latency and energy compared to repeaters. A series coupling capacitance offers pre-emphasis to lower wire delay, reduces the driven load, and lowers the wire voltage swing without a second power supply. A 0.18µm CMOS testchip shows 10.5× energy savings at a 50mV swing compared to full-swing repeated wires, and a 3× gain in wire bandwidth.

22.9 A 0.28pJ/b 2Gb/s/ch Transceiver in 90nm CMOS for 10mm On-Chip Interconnects **12:00 PM**

E. Mensink, University of Twente, Enschede, The Netherlands

A low-swing transceiver for 10mm-long 0.54µm-wide on-chip interconnects is presented. A capacitive pre-emphasis transmitter lowers the power and increases the bandwidth. The receiver uses DFE with a power-efficient continuous-time feedback filter. The transceiver, fabricated in 1.2V 90nm CMOS, achieves 2Gb/s. It consumes 0.28pJ/b, which is 7× lower than earlier work.